WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having an element region; and

an element isolation region formed around the element region, the element isolation region being formed of an insulation material having a higher thermal expansion coefficient than the element region.

2. The semiconductor device according to claim 1, wherein the semiconductor substrate has an SOI structure.

3. The semiconductor device according to claim 1, wherein the element isolation region is formed of SiN.

4. The semiconductor device according to claim 3, wherein the element isolation region has a trench formed around the element region, and an SiN layer formed in the trench.

5. A semiconductor device comprising:

a semiconductor substrate having an element region; and

an element isolation region formed around the element region, the element isolation region having a first layer and a second layer, the first layer being formed of an insulation material and located in contact with the element region, the second layer being located inside the first layer and formed of a conductive material, the conductive material having a thermal

expansion coefficient higher than a thermal expansion coefficient of the element region.

6. The semiconductor device according to claim 5, wherein the semiconductor substrate has an SOI structure.

7. The semiconductor device according to claim 5, wherein the conductive material is a metal.

8. The semiconductor device according to claim 7, wherein the conductive material is one selected from the group consisting of Al, Cu, TiN, Ti, W, TaN, Co and Ni.

9. The semiconductor device according to claim 5, wherein the conductive material is a salicido-based material.

10. The semiconductor device according to claim 9, wherein the conductive material is one selected from the group consisting of TiSi, TiSi2, CoSi, CoSi2 and NiSi, NiSi2.

11. The semiconductor device according to claim 5, wherein the insulation material is SiN.

12. A semiconductor device comprising:

a semiconductor substrate;

a first element region formed in the semiconductor substrate, a gate electrode being provided on the first element region, source and drain regions being formed in the first element region;

an element isolation region provided around the

first element region; and

recesses formed in opposing sides of the first element region, the element isolation region being formed in the recesses.

13. The semiconductor device according to claim 12, wherein the opposing sides of the first element region oppose each other in a direction of a channel length.

14. The semiconductor device according to claim 12, wherein the opposing sides of the first element region oppose each other in a direction of a channel width.

15. The semiconductor device according to claim 13, wherein a length of the recesses in a direction of a channel width is longer than a distance between the first element region and a second element region provided separate from the first element region in the direction of the channel width.

16. The semiconductor device according to claim 14, wherein a length of the recesses in a direction of a channel length is longer than a distance between the first element region and a third element region provided separate from the first element region in the direction of the channel length.

17. The semiconductor device according to claim 12, wherein the element isolation region is

formed of a material having a lower thermal expansion coefficient than a material of the first element region.

18. The semiconductor device according to claim 12, wherein the first element region is formed of Si, and the element isolation region is formed of SiO_2.

19. The semiconductor device according to claim 12, wherein the semiconductor device is an N-type semiconductor device.

20. The semiconductor device according to claim 12, wherein the semiconductor substrate has a relaxed layer, the first element region and the element isolation region being provided on the relaxed layer, the first element region being formed of strained-Si, the element isolation region being formed of SiO_2, the semiconductor device being a P-type semiconductor device.